Vol. 4.Special Issue ICCSII ISSN 2079-8407
Journal of Emerging Trends in Computing and Information Sciences

http://www.cisjournal.org

A Reduced-Complexity Fast GPS Receiver using a Systolic Architecture

[1]Yassine SALIH-ALJ, [2]François GAGNON, [3]René Jr. LANDRY

[1] School of Science & Engineering, Al Akhawayn University in Ifrane, PO. Box. 2134, Ifrane 53000, Morocco.

[2,3] Electrical Engineering Department, École de Technologie Supérieure, 1100, Notre-Dame W. Montreal (Qc) H3C 1K3 Canada.

E-mail: [1] Y.Alj@aui.ma, [2] Francois.Gagnon@etsmtl.ca, [3] Rene.Landry@etsmtl.ca

ABSTRACT

This paper presents a new structure for fast GPS receivers. The suggested GPS acquisition scheme leverages a systolic-based array structure of regular and simple locally-connected processing-elements (PEs). The new GPS system is simulated and its complexity is evaluated for a real-time implementation on a field programmable gate array (FPGA). The proposed systolic-based acquisition system promises high performance for GPS receivers by yielding greatly improved processing latency and estimation precision while offering an efficient and flexible implementation of a significantly reduced complexity of a fully pipelined architecture.

Keywords: *GPS, acquisition, digital signal processing, FPGA implementation.*

1. INTRODUCTION

Global Positioning System (GPS) has become much more solicited and even essential in several applications as for aircraft positioning, smart missile systems, automated guided vehicles and other civilian applications. The increasing number of applications commonly using navigation instruments (i.e., GPS receivers) has maintained over the past two decades a significant research interest for these systems. A GPS receiver performs ranging measurements with respect to NAVSTAR (Navigation Satellite Timing and Ranging) satellites to determine its position, velocity, and timing information [1], [2]. The distance from the receiver to each of the acquired satellites is calculated as the multiplication of the corresponding measured propagation time and the speed of light. Correlation between each acquired satellite's unique PRN (Pseudo Random Noise) code and its corresponding locally-generated C/A replica is computed to measure the propagation time by estimating the code-shift τ used for ranging measurements. Gold code is used for its correlation properties of highly peaked autocorrelation and minimum cross-correlation.

Indeed, timing acquisition is the most costly operation in the GPS receiver [2]; hence an efficient acquisition process is required for even faster and computationally-reduced receiver's architecture. The acquisition time which is regarded as the key factor for GPS receivers, is not defined only by the processing technique but also by the selected correlation method. For a traditional acquisition system that requires for its time-domain correlation N^2 multiplications and N^2-1 addition operations (where N is the number of data samples) [3], the resulting computational burden can be very high compared to an FFT-based acquisition system. Indeed, the acquisition time is exponentially reduced (as the number of data samples increases) for a frequency-domain correlation characterized by a greatly improved complexity of approximately $2N\cdot\log_2 N+N$ multiplications and $2N\cdot\log_2 N$ additions [4], [5]. The use of FFT for accelerating the GPS acquisition process has been the topic of extensive study [5]-[12]. However, though their computational efficiency, FFT-based GPS receivers (that use power-of-two lengths) have some sampling constraints of sequence lengths owing to Gold code that requires using some averaging techniques for such frequency-domain processing [6], [8].

The arising question remains if one can simply accelerate the correlation computation in time domain using a method that explicitly reduces the number of operations. Indeed, a simpler correlation technique is required for a faster GPS acquisition using flexible and modular structure that reduces the acquisition time and makes real-time processing feasible. A modular processing that has the potential for very high speed applications is inherently suitable for a fully pipelined implementation on a field programmable gate array (FPGA). This paper mainly focuses on reducing the computational burden of signal acquisition and suggests an efficient modular structure to shorten the acquisition time. Systolic designs represent a popular architectural model for efficient and flexible implementation of computationally intensive digital signal processing (DSP) applications [13]. This owes to the simplicity of such design that rhythmically uses identical processing elements (PEs) with local and regular interconnections, enabling the inherent potential of using a high level of pipelining in a VLSI implementation. The suggested GPS scheme in this paper uses the systolic-based modular processing paradigm that is efficiently supported for an FPGA implementation.

The remainder of this paper is organized as follows. In Section 2, systolic design principles are briefly presented. In Section 3, a derivation of a systolic GPS correlator is discussed, and development of the proposed systolic-based GPS acquisition system is described in Section 4. The computational gain in complexity of the proposed architecture is estimated and compared with the corresponding FFT-based structure, and its hardware implementation on different *Xilinx* FPGAs is detailed in Section 5. Finally, Section 6 concludes the paper.

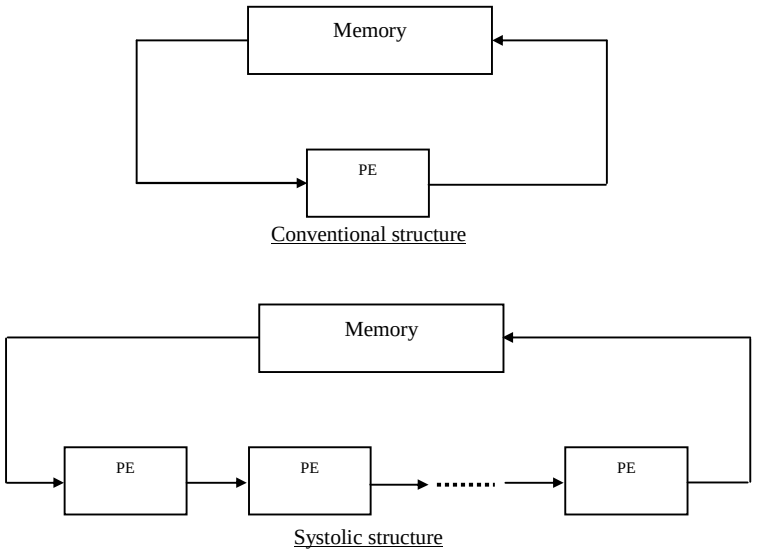

Fig 1: Systolization mechanism.

2. SYSTOLIC DESIGN PRINCIPLES

The principle of a systolic architecture was introduced in 1978 by Kung and Leiserson [14]. It consists of replacing a global processing element (PE) by a regular array of identical and simple processing elements, called cells, which are locally interconnected as shown in Figure 1 [13]. This technique involves a fascinating interplay between architectural and algorithmic aspects. Thus an architecture involving local communication and pipelined processing is well suited for FPGA implementation.

A memory or, generally, a host station is responsible for communications between the systolic array and its external environment. Once an external data is received by a cell at the array's borders, it is pumped from a cell to cell along the systolic array. Each cell receives data from the previous cell, calculates and transmits it on the next clock cycle to the following cell. Therefore, the data is processed in the systolic array with a constant speed, obviously the data arrival speed.

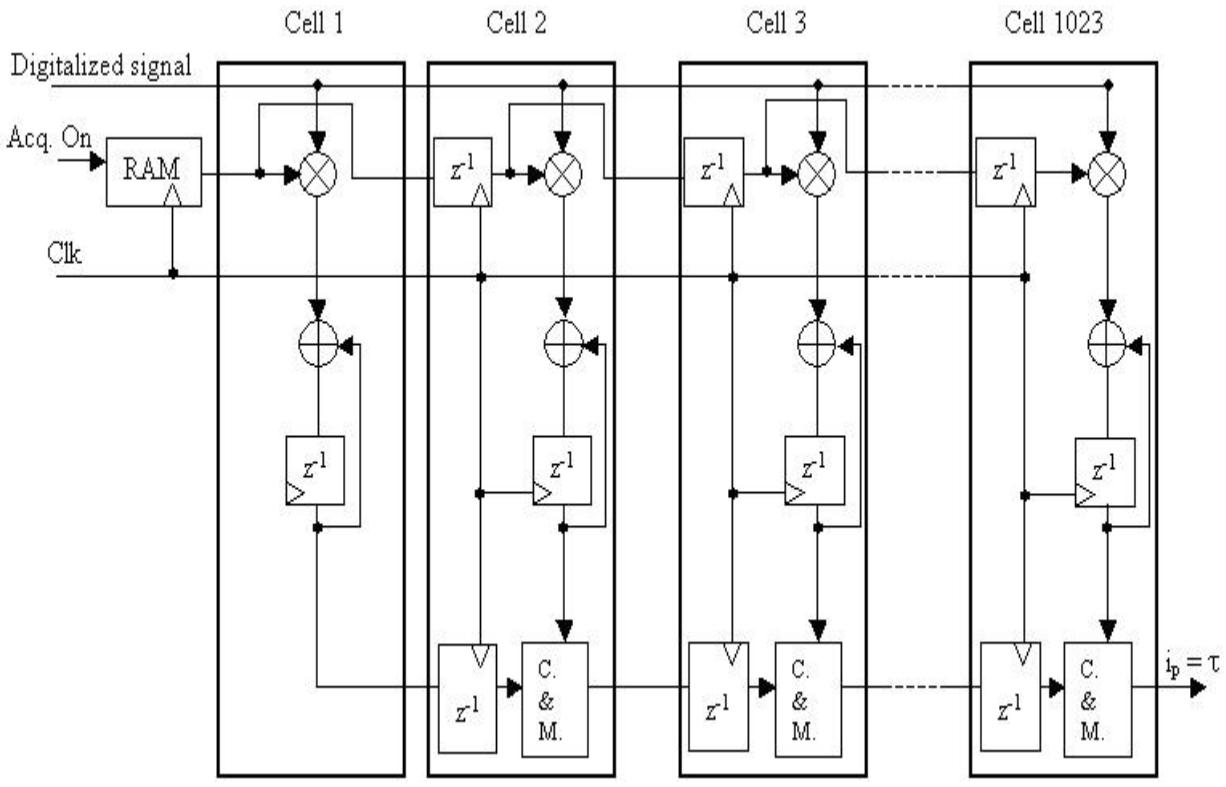

Fig 2: Block-diagram of the proposed systolic-based GPS code correlator.

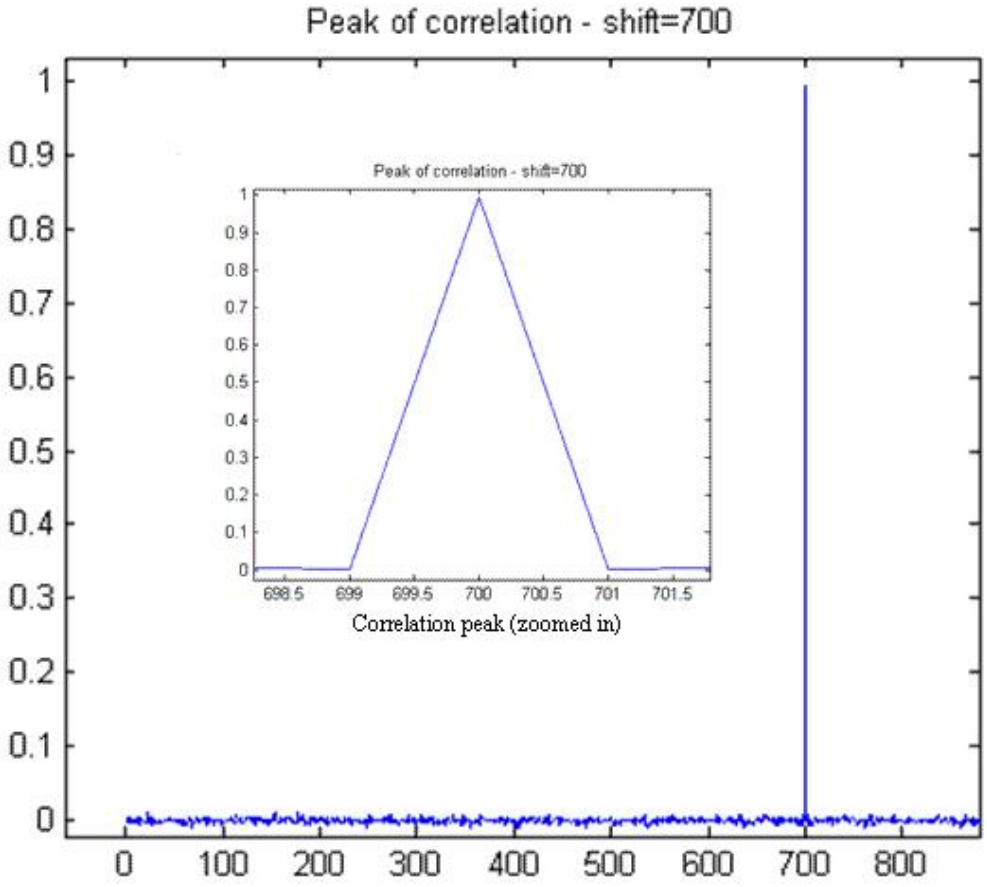

Fig 3: Obtained correlation peak for a code-shift of 700 chips.

3. SYSTOLIC GPS CORRELATOR

A systolic structure is adopted for mapping the GPS correlator architecture. This initially requires determining the necessary number of PEs in the corresponding systolic array. Indeed, the C/A code length of 1023 chips corresponds to the minimum number of required cells in a systolic array that is controlled by a clock of 2.046 MHz (two samples per chip per cell). The obtained precision for the estimated code-shift τ is hence directly related to the used number of cells. Obviously, the more cells are used, the better resolution is obtained for this estimation.

The block-diagram of the considered GPS code correlator is illustrated in Figure 2. For peak detection, each PE evaluates its corresponding greater accumulated value using a sign multiplication, an accumulator and a comparator C&M that memorizes the corresponding cell's index i. This value is compared from a cell to its subsequent updating the greatest value that represents the obtained correlation peak and hence deducing from its location (of the corresponding index ip) the estimated code-shift τ in terms of chips. Furthermore, each of the used z-1 delays is obviously synchronized to half of the C/A code chip length Tc/2 (Shannon theorem). The accumulation result Ri for each cell of the systolic array can be expressed as:

$$R_i = \sum_{j=0}^{N-i+1} s(j) \cdot c(j+i-1), \qquad (1)$$

where s(j) is the digitalized received signal, c(j) is the C/A code replica and N is the number of the processed samples (i.e., chips) by the systolic array. The processing time required for detecting the searched peak of correlation is theoretically one C/A code period length of 1 ms. Hence, the minimum number of samples N would be 2046 in accordance with two times the corresponding number of chips for a C/A code period. Figure 3 shows the obtained correlation peak for a code-shift of 700 chips when plotting each consecutive accumulated value Ri corresponding to each cell i.

Indeed, the proposed systolic-based GPS code correlator estimates the code-shift τ that corresponds to the cell ip responsible of the obtained maximum correlation peak. However, for dynamic GPS applications a Doppler offset is also considered as the received signal is complex and is divided between in-phase I and quad-phase Q components. The considered acquisition process should also estimate this frequency phase besides the code-shift.

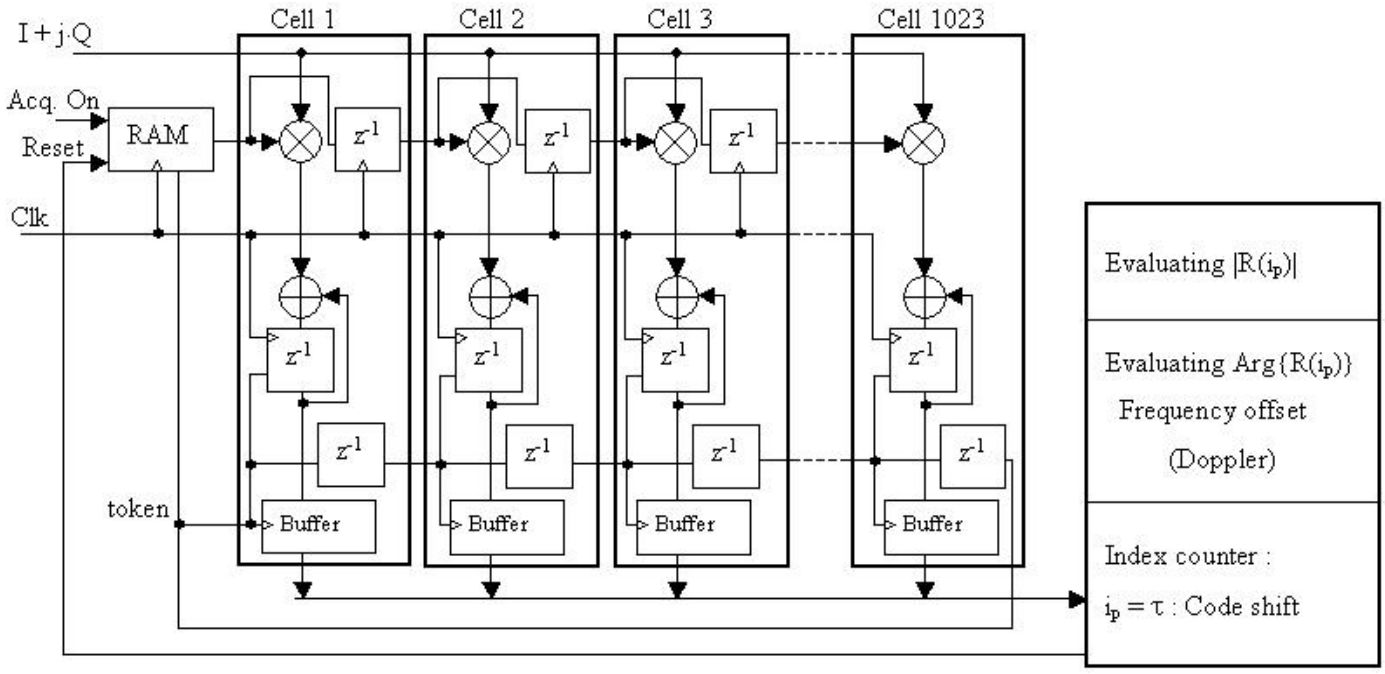

Fig 4: Block-diagram of the suggested systolic-based GPS fast acquisition system.

4. SUGGESTED SYSTOLIC-BASED ACQUISITION SYSTEM

To acquire a complex signal characterized by a frequency phase, the Doppler offset must be evaluated. Hence, for a complete GPS signal acquisition, the considered acquisition system should determine the carrier phase ϕ that represents the argument of the corresponding complex peak of correlation R(τ) as:

$$\phi = \arg\{R(\tau)\} = \arctan\left(\frac{Q}{I}\right). \qquad (2)$$

While the correlation function modulus for a code-shift τ, gives the correlation peak value as:

$$A_{\max} = |R(\tau)|. \qquad (3)$$

Indeed, a complete GPS acquisition system is considered based on the systolic correlator and a simple estimation module which evaluates τ, ϕ, and Amax. The block-diagram of this suggested acquisition system is illustrated in Figure 4. The shown systolic array structure was further improved by replacing the comparators C&M with buffers at the cells' outputs. These buffers are controlled by a token which allows communicating the accumulated values, by each cell, to the estimation module.

This module estimates code and frequency deviations besides correlation peak magnitude. The modulus of each accumulated value |R(ip)| is continuously compared and updated. If it is found greater than its latter, a new Doppler phase is estimated by (2) using an efficiently fast arctangent approximation:

$$\phi \approx \frac{Q/I}{1 + 0.28125\left(Q/I\right)^2} \text{ radians}, \qquad (4)$$

which has surprisingly good performance of a maximum error as low as 0.26 degrees [15].

Furthermore, during the acquisition process, the peak is simultaneously searched by evaluating its maximum amplitude through the 1023 chips, and determining its corresponding position ip (using a counter which counts from 1 to 1023). The used token also serves to reset each cell's accumulator after a complete processed period of 1023 chips. The considered estimation module controls the systolic array by a reset signal that leads the Read Access Memory (RAM) index to the next satellite's corresponding C/A replica. For the considered systolic array (of Figure 4) that considers 1023 cells, the code phase resolution is within half of a chip. Indeed, a further refined estimation can be obtained by simply increasing the number of used PEs in the corresponding systolic array. This involves using shorter time delays z-1 for a maintained C/A propagation period of 1 ms, e.g., as for an array of 2046 cells the used delays should be controlled by a clock period of Tc/4.

The simplicity and the resulting efficient architecture that characterize this proposed modular systolic-based GPS acquisition system motivate for a real-time implementation in a reconfigurable platform such as an FPGA. Indeed, such optimum and easily available solution is clearly advantageous for its provided flexibility (as in software) and for its high performance (as in ASIC) that promises a reduced acquisition time.

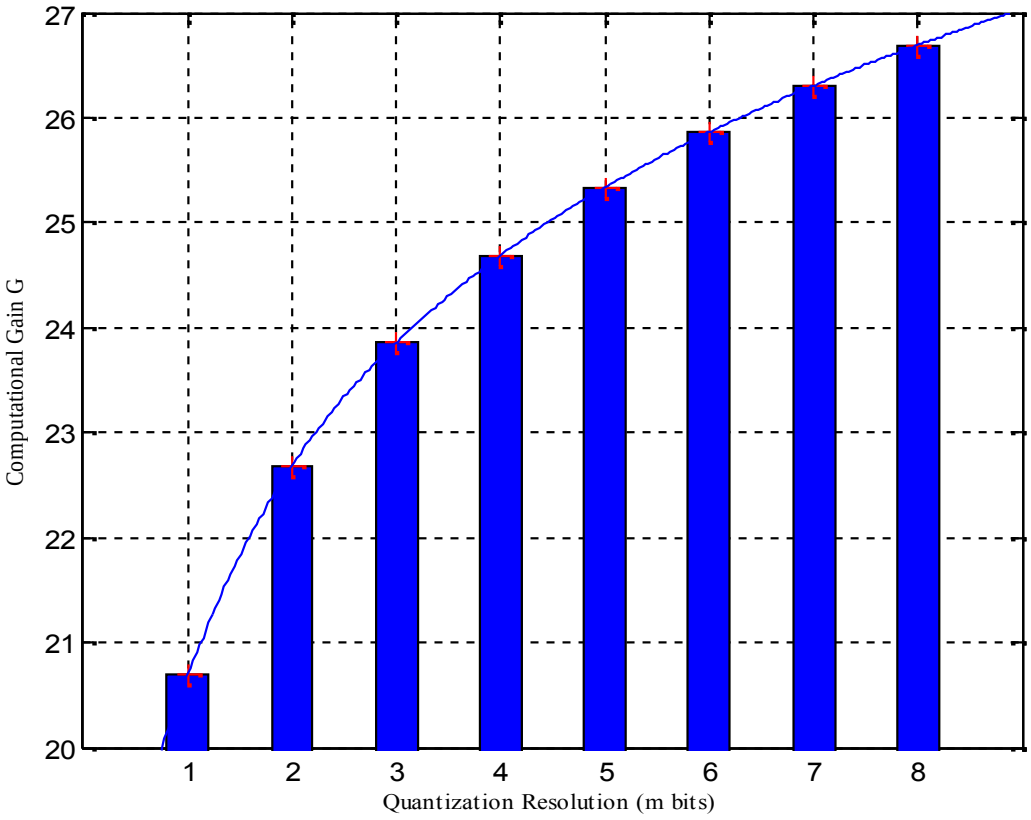

Fig 5: Gain in complexity with respect to the quantization resolution.

5. HARDWARE COMPLEXITIES FOR AN FPGA IMPLEMENTATION

Indeed, using systolic processing concept along with digital design techniques in a reconfigurable platform such as an FPGA would be an optimum and easily available solution.

The suggested GPS acquisition system based on the considered systolic structure is mainly made up of PEs. These elements are simple and identical to each other. Each of the Nc cells has three delay blocks, a buffer, a complex addition and multiplication. Indeed, the considered GPS acquisition scheme is distinguished by this systolic-based correlator as the most sizeable and important operation for GPS signals acquisition. Hence, the obtained computational complexities in terms of the total number of required addition/multiplication operations and necessary bits to memorize of the proposed systolic realization along with the existing systems are listed in Table 1.

It is found that the proposed systolic-based scheme involves significantly less number of adders and multipliers compared to the FFT-based acquisition scheme [12] and the time-domain traditional system [3], but with more memory resources that are amply available on each slice of recent FPGAs' generations, e.g., Each Virtex-6 FPGA slice contains eight flip-flops and four LUTs (Look-Up-Tables) [20].

Table 1: Computational Complexities of the Proposed Sytolic-based GPS Scheme and the Traditional and FFT-based GPS Acquisition Systems.

Cost \ Systems	Traditional System [3]	FFT-based System [12]	Systolic-based Scheme
Additions	N_c^2-1	$2(N_c+1)\log_2(N_c+1)$	N_c
Multiplications	N_c^2	$2(N_c+1)\log_2(N_c+1)+ N_c+1$	N_c
Memory Bits	N_c	N_c+1	$2N_c$

In the prospect of a practical implementation of the proposed GPS systolic-based scheme, the related design complexity is analyzed with respect to current VLSI (Very-Large-Scale Integration) chips for a given quantization level. Indeed, for an acceptable to a very minimized SNR (Signal-to-Noise Ratio) degradation of GPS signal, the corresponding quantization size ranges respectively from 1-bit to 8-bit resolution [16], [17]. A maximum of 8-bit quantization is therefore considered in this paper for the design complexity evaluation. Assuming that a multiplication computation takes as much as two addition operations, then the obtained gain in complexity of this proposed systolic-based GPS acquisition scheme in comparison to an FFT-based scheme is illustrated in Figure 5 in terms of the used quantization resolution.

Accordingly, the obtained computational gain G can be modeled in terms of the used quantization resolution m as

$$G = 8.1 \cdot 10^{-4} \cdot m^5 - 2.2 \cdot 10^{-2} \cdot m^4 + 0.24 \cdot m^3 - 1.4 \cdot m^2 + 17. \quad (5)$$

We note for a quantization resolution of 8 bits, a significant reduction in the computational cost by a factor of almost 27. Consequently, the acquisition time is considerably improved with such computational cost reduction.

For an implementation on recent Virtex series of Xilinx's FPGAs, arithmetic functions can be performed through the FCL (Fast Carry Logic) available on the slices, respectively, in 4 bits and 2 bits per slice for Virtex-6/Virtex-5 and their previous generations (i.e., Virtex-II Pro/Virtex-4) [18], [19], [20], [21]. However, since a 9-bit result is obtained for an 8-bit addition if a carry is allowed, then the corresponding cost in terms of slices on Virtex-II Pro/Virtex-4 and Virtex-5/Virtex-6, is respectively, the following:

$$\frac{1\,slice \times 9\,bits}{2\,bits} = 4.5\,slices, \quad (6)$$

$$\frac{1\,slice \times 9\,bits}{4\,bits} = 2.25\,slices. \quad (7)$$

Similarly, the 16-bit result obtained by an 8-bit multiplication, corresponds to the following:

$$\frac{1\,slice \times 16\,bits}{2\,bits} = 8\,slices, \quad (8)$$

$$\frac{1\,slice \times 16\,bits}{4\,bits} = 4\,slices. \quad (9)$$

Consequently, the total complexity in terms of slices with respect to the used FPGA generation and quantization resolution is presented in Table 2.

Table 2: Total Complexity in terms of Slices.

Complexity in slices \ Resolution	**4-bit**	**8-bit**
Virtex-II Pro / Virtex-4	16 368	29 667
Virtex-5/Virtex-6	9 718	14 834

Notice that only 60 kilobits (i.e., 2 kilobits per satellite) are needed in terms of RAM resources in the used FPGA to memorize the 30 NAVSTARs' local C/A code replicas. If we consider for a 4-bit quantization the XC4VLX40 Virtex-4 chip that offers a maximum number of slices of 18,432 and a 1,728 kilobits of RAM resources [19], the suggested systolic-based correlator requires then for its implementation less than 89 % and 3.5 % of these resources, respectively.

For an 8-bit resolution, if we consider for instance, the Virtex-5 XC5VFX100T chip [20], with a preserved clock rate of 2.046 MHz, an optimal implementation of the considered system would use less than 93 % and 0.8 % of slices and RAM resources, respectively.

Moreover, this complexity in terms of slices can be further reduced when considering the embedded IBM PowerPC processors available on this chip. Thus, smaller chips could be used for more compact and optimized complexity.

Furthermore, considering the high processing speed that characterizes modern Xilinx's FPGAs, a faster internal clock rate of about 200 MHz would allow implementation of the suggested system in the smallest Virtex-4 chip, i.e., XC4VFX12, as shown in Table 3. Indeed, this can be achieved by using a simple block processing strategy that would allow storing the incoming bits in buffers to be then fed to a reduced number of cells in the corresponding systolic array. For a preserved constant time response with a condensed array of 100 cells, a ten times faster clock should be used with a such reduced complexity by a factor of 10. Therefore, considering a block processing strategy for the suggested flexible systolic-based architecture would yield a further improved processing speed with a flexible implementation characterized by an efficiently reduced complexity of a fully pipelined architecture.

Table 3: Implementation Cost of the Suggested Systolic-based GPS System on Virtex's FPGAs for an 8-bit Quantization.

Virtex's FPGAs	**Clock Rate / Cost**	***F* =2.046 MHz ~ 2 MHz**	**10^{1}×*F* ~ 20 MHz**	**10^{2}×*F* ~ 200 MHz**
XC6VLX760	Slices	12.51 %	1.25 %	0.12 %
	RAM	0.23 %	0.23 %	0.23 %
XC5VFX100T	Slices	93 %	9.3 %	0.93 %
	RAM	0.8 %	0.8 %	0.8 %
XC4VFX12	Slices	-	54.21 %	5.42 %
	RAM	-	9.25 %	9.25 %

6. CONCLUSION

In this paper, a new structure has been proposed for GPS receivers. The considered GPS acquisition system leverages systolic-based linear array architecture of simple and identical locally-connected cells. The suggested GPS scheme of a fully pipelined architecture is naturally suitable for a real-time implementation on FPGAs. While promising high performance for GPS receivers, the considered systolic-based acquisition system offered a greatly improved processing latency through a significantly reduced hardware complexity in comparison with the existing structures of GPS receivers. The systolic-based structure is found to have a nearly 27 times lower area-time complexity in comparison with fast FFT-based structures and has involved an efficient implementation on Virtex's FPGAs. Therefore, this proposed GPS scheme is regarded as being an excellent solution for fully pipelined architectures of current GPS receivers.

REFERENCES

[1] E. D. Kaplan, ed., Understanding GPS: Principals and Applications, Artech House Publishers, 1996.

[2] M. S. Braasch and A. J. Dierendonck, "GPS Receiver Architectures and Measurements," Proc. IEEE, Vol. 87, No.1, pp.48-64, Jan. 1999.

[3] J. G. Proakis and D. G. Manolakis, Digital Signal Processing, Principles, Algorithms and Applications, Prentice Hall, 1996.

[4] W. Smith and J. Smith, Handbook of Real-Time Fast Fourier Transforms, IEEE Press, 1995.

[5] D. Van Nee and A. Coenen, "A new fast GPS code acquisition technique using FFT," Electronic Letters, Vol. 27, pp. 158-160, Jan. 1991.

[6] C. Yang,"Fast code acquisition with FFT and its sampling schemes," Proc. ION, GPS-96, Kansas City, MO, Sep. 1996.

[7] N. F. Krasner, "GPS receiver and method for processing GPS signals," USA patent, PN 5,781,156, Jul. 1998.

[8] J. A. Starzyk and Z. Zhu, "Averaging correlation for C/A code acquisition and tracking in frequency domain," Proc. of the IEEE Midwest Symposium on Circuits and Systems, Vol. 2, Aug. 2001.

[9] A. Alaqeeli, J. Starzyk, and F. Van Graas, "Real-time acquisition and tracking for GPS receivers," Proc. of the IEEE International Symposium on Circuits and Systems, Vol. 4, May 2003.

[10] D. Akopian, "Fast FFT based GPS satellite acquisition methods," Proc. of IEE Radar Sonar Navig., Vol.152, No. 4, PP. 277-286, Aug. 2005.

[11] C. Sajabi, C.-I. H. Chen, D. M. Lin and J. B. Y. Tsui, "FPGA frequency domain based GPS coarse acquisition processor using FFT," Proc. of IEEE Instrumentation and Measurement Technology Conference, pp. 2353-2358, Apr. 2006.

[12] S. R. Babu, P. Selvam, G. S. Rao, and W. Jinling, "Optimization of GPS L1 acquisition using Radix-4 FFT," Proc. the IEEE International Conf. on Recent Trends in Information Technology (ICRTIT'11), pp. 875-879, Jun. 2011.

[13] H. T. Kung, "Why systolic architectures?," Proc. of Computer Magazine, Vol. 15, No. 1, pp. 37-45, Jan. 1982.

[14] H. T. Kung and C. E. Leiserson, Algorithm for VLSI Processor Arrays, In Introduction to VLSI systems, Chapter 8.3, Addison-Wesley, 1980.

[15] R. G. Lyons, "Performing efficient arctangent approximation," in EE|Times Design, Jun. 2011.

[16] A. Schmid, "Semiconductor implementation of differential correlation and noncoherent integration," International Global Navigation Satellite Systems Society Symposium IGNSS'07, Dec. 2007.

[17] S. Hickling, "Sampling quantization for GPS or GNSS RPS systems," Spirent ebook, Mar. 2011.

[18] E. Garcia, "Desinging properly with FPGAs," MVD Company Electronic Publications, No. 125, pp. 2–6, May 2002.

[19] Xilinx inc., "Virtex-4 Family Overview," Aug. 2010. URL: http://www.xilinx.com/support/documentation/data_sheets/ds112.pdf

[20] Xilinx inc., "Virtex-5 Family Overview," Feb. 2009. URL: http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf

[21] Xilinx inc., "Virtex-6 Family Overview," Jan. 2012. URL: http://www.xilinx.com/support/documentation/data_sheets/ds150.pdf

AUTHOR PROFILES

Yassine Salih-Alj received the Bachelor's degree in microelectronics from the University of Quebec at Montreal (UQAM), Montreal, Quebec, Canada, in 2001, and the Master's degree in electrical engineering from the École de Technologie Supérieure (ETS), Montreal, Quebec, Canada, in 2003, and the Ph.D. degree in Telecommunications from the National Institute of Scientific Research - Energy, Materials & Telecommunications (INRS-Telecom), Montreal, Quebec, Canada, in 2008. He served as a research assistant at the Telebec Underground Communications Research Laboratory (LRTCS) from 2005 to 2008, and then during 2009 as a Postdoctoral Fellow at Poly-Grames Research Center, of the École Polytechnique de Montréal, Montreal, Quebec, Canada. He is currently working as a permanent faculty member at the School of Science and Engineering (SSE) of Al Akhawayn University in Ifrane (AUI), Morrocco.

François Gagnon received the B.Eng. and Ph.D. degrees in electrical engineering from École Polytechnique de Montréal, Montréal, PQ, Canada. Since 1991, he has been a professor in the Department of Electrical Engineering, École de Technologie Supérieure, Montréal, Canada. He chaired the department from 1999 to 2001 and is now the holder of the Ultra Electronics (TCS) Chair in wireless communication at the same university. His research interest covers wireless high speed communications, modulation, coding, high speed DSP implementations, and military point to point communications. He has been very involved in the creation of the new generation of high capacity line of sight military radios offered by the Canadian Marconi Corporation, which is now Ultra Electronics Tactical Communication Systems.

René Jr. Landry received a B.E. degree at the École Polytechnique de Montreal, Canada in 1992, a M.S. in satellite communication engineering at the University of Surrey, Guildford, England in 1993, a master in space electronics and a DEA in microwaves at the ENSAE/SupAero, Toulouse, France in 1994. He obtained his Ph.D. degree at Université Paul-Sabatier, Toulouse, France in 1997. He also received a Post Doc in Space Science at the National French Space Industry (CNES), Toulouse, France, in 1998. Since 1999, he has been involved in the problem of GPS/Galileo/Bluetooth

Interferences for the Canadian navigation and communication industries. His major interest concerns the development of new innovative mitigation techniques for GPS receiver robustness design including those of electronic inertial navigation system based on low cost MEMs. He is actually working on several digital signal processing applications in satellite navigation, anti-jamming and inertial navigation system.